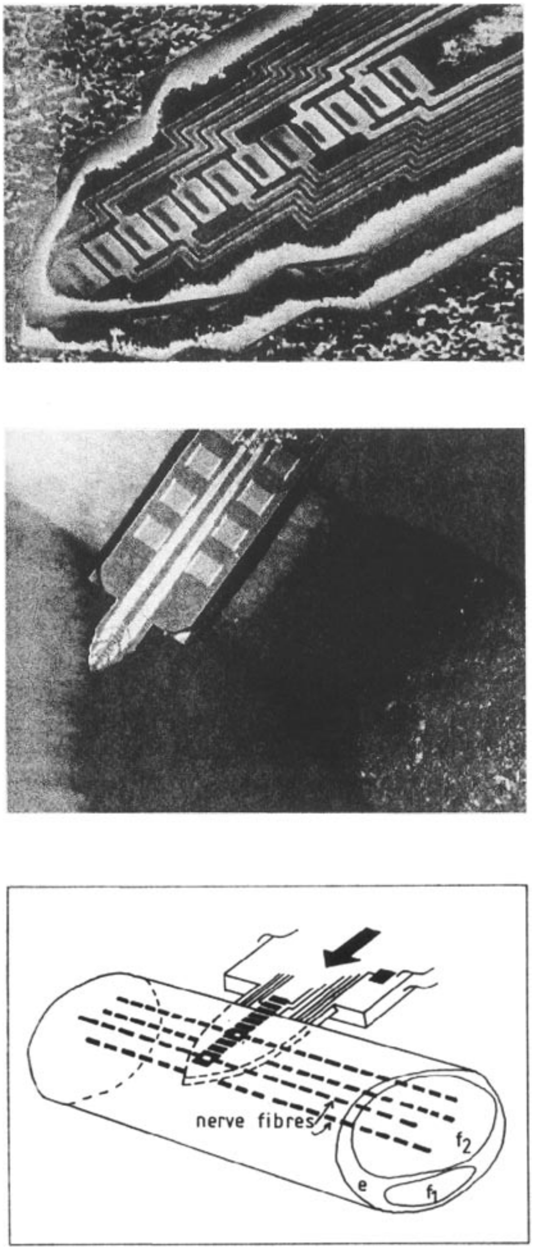


Figure 12 (*top*) 1-D silicon tip-shaped array with 12 platinum electrode sites 50 × 50 μm at a distance of 50 μm from each other. Insulation layer is Si_3N_4, tip thickness is 60 μm. (*middle*) The device against the tip of a match. (*bottom*) Insertion of the tip device into fascicle f2 of a typical peroneal nerve trunk of a rat (diameter 0.5 mm) (from Ref. 26).

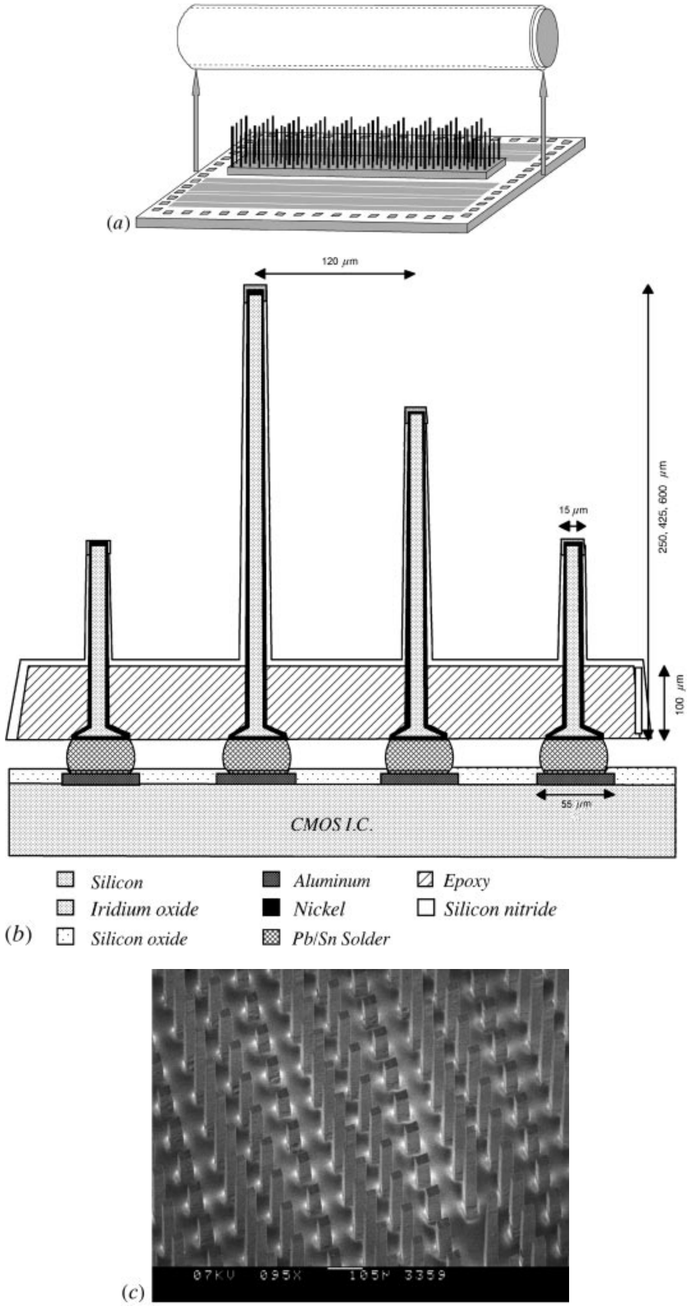


Figure 15 (*a*) Scheme of the University of Twente 128-electrode 3-D glass-silicon array (UT-128 array), mounted on a CMOS, mixed mode processing chip with dimensions 4×4 mm. Needle length is 600, 425, or 250 μm; width at tip is 15 μm; and needle spacing is 120 μm. (*b*) Details of the dimensions and materials used for the UT-128 array. (*c*) A "sea" of sawn and etched silicon needles of three different lengths, embedded in a glass matrix.

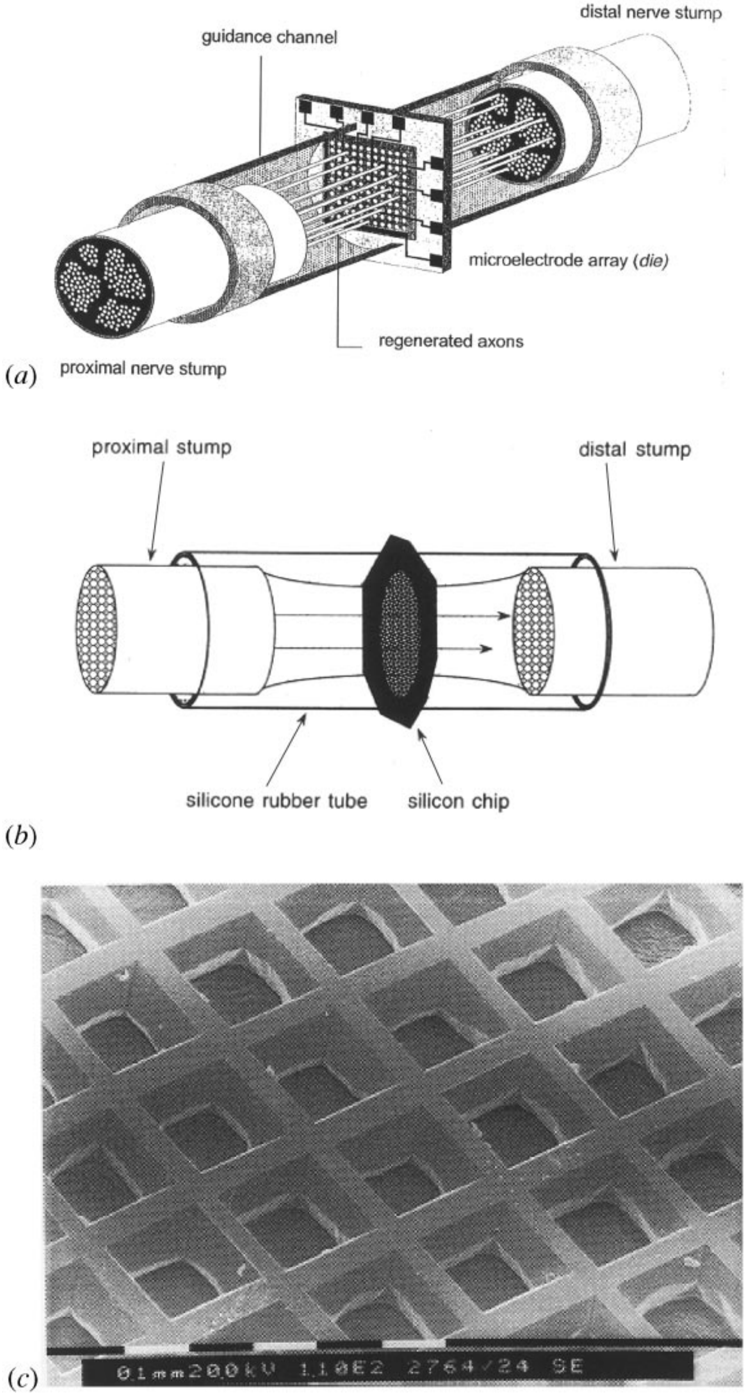


Figure 18 (*Continued*)

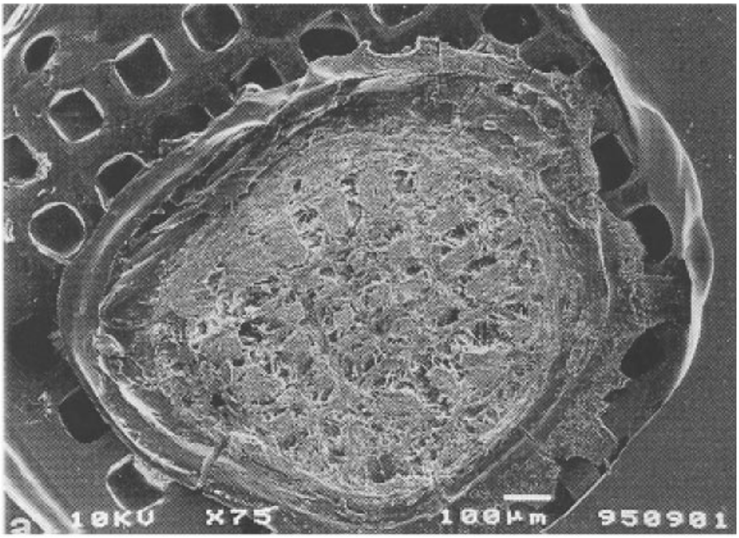
(*d*)


Figure 18 (*a*) Schematic representation of an intelligent neural interface (sieve array) implanted into an intersected nerve (from Ref. 71, Figure 1). (*b*) Schematic drawing of the silicone chamber model with the inserted silicon chip bridging a 4-mm gap between the proximal and distal stumps of a transected rat sciatic nerve. (from Ref. 70, Figure 3). (*c*) Detail of the sieve. SEM photograph of a fabricated chip with 100-μm diameter holes (from Ref. 70, Figure 2). (*d*) SEM photograph of nerve tissue sections distal to a chip with hole diameters of 100 μm after 16 weeks of regeneration. Shown is a minifascicular pattern on the distal surface of the chip. The regenerated nerve structure has a smaller diameter than that of the perforated area of the chip. The circumferential perineural-like cell layer is clearly visible (from Ref. 70, Figure 5, *top*).