Room temperature operation of a single electron transistor made by the scanning tunneling microscope nanooxidation process for the TiO_x/Ti system

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The single electron transistor (SET) is fabricated using the scanning tunneling microscope (STM) as a fabrication process, and the fabricated SET operates at room temperature. Using the STM tip as a cathode, the surface of the titanium metal can be oxidized, and the few tens of nanometer wide oxidized titanium line can be made. The small island region of the SET of $\sim 30\times\sim 35$ nm^2 is formed by the oxidized titanium line. The Coulomb staircase of 150 mV period is observed in the current–voltage characteristics of the SET at room temperature. © *1996 American Institute of Physics.* [S0003-6951(96)00101-2]

Recently, a single electron transistor (SET) is considered to be a candidate for an element of a future low power, high density integrated circuit because of a possible ultralow power operation with a few electrons. For the practical application it is indispensable for the SET to be operated at room temperature. For this purpose, the size of the island of SET must be as small as $\sim$10 nm to reduce the total capacitance of SET and to overcome the problems of the thermal fluctuation. However, the size of $\sim$10 nm is out of the range of the present conventional microfabrication process. Therefore, instead of using an artificial pattern formation method, the self-organized small size structure such as a thin polysilicon film was used for the small island and the room temperature operation of the single electron memory was realized.[1] However, the controllability of the size and the structure of the island of the SET is quite difficult in such spontaneous size formation method.

In this letter, we present the fabrication of an SET using a new artificial pattern formation method based on the scanning tunneling microscope (STM) nano-oxidation process for the first time, which we established.[2] The SET operates at room temperature, showing a clear Coulomb staircase of $\sim$150 mV period even at 300 K.

The principle of the STM nano-oxidation process[2,3] is shown in Fig. 1. A 3 nm thin titanium (Ti) metal is deposited by the evaporation on the thermally oxidized SiO_2 (100 nm)/ *n*-Si substrate. The Ti surface was oxidized by anodization using the STM tip as a cathode through the water that adhered to the surface of Ti from the atmosphere, and the oxidized titanium (TiO_x) line of nanometer size was formed. The barrier height of the TiO_x/Ti is found to be 285 meV for the electron from the temperature dependence of the current.[3] The relative permittivity of the TiO_x is found to be $\epsilon_r=24$ from the electric field dependence of the TiO_x barrier height.[4] Using the TiO_x/Ti system, SET is fabricated.

Figure 2 shows the schematic illustration of the SET made by the STM nano-oxidation process. At both ends of the 3 nm thick Ti layer, the source and drain ohmic contacts are formed by depositing Ti/Au pad metal, and at the backside of the *n*-Si substrate, the gate ohmic contact is formed by depositing the aluminum metal. At the center region of the Ti layer the island region is formed, which is surrounded by the two parallel narrow TiO_x lines that will work as tunneling junctions for the SET and the two large TiO_x barrier regions as shown in Fig. 3, which is an atomic force microscopy (AFM) image of the island region of the fabricated SET. These TiO_x lines and the large TiO_x barrier regions are made by the STM nano-oxidation process.

The typical size of the TiO_x line is 15–25 nm wide times 30–50 nm long. The island size is 30–50 nm times 35–50 nm. The most important feature of this structure is that the tunnel junction area that corresponds to the cross section of the TiO_x line is as small as 2–3 nm (the thickness of the Ti layer) times 30–50 nm (the length of the TiO_x line). The deposited Ti layer is as thin as 3 nm, and the surface of the Ti layer is spontaneously oxidized about $\sim$1 nm. Therefore, the intrinsic Ti layer thickness is considered to be less than 3 nm. Owing to this small tunneling junction area, the tunnel capacitance becomes as small as the order of 10^{-19} F, which leads the SET to be operated at room temperature as will be shown in the following.

The current–voltage characteristics of the single electron

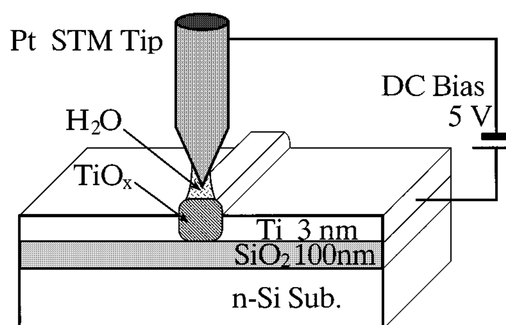

FIG. 1. Principle of STM nano-oxidation process using STM tip as cathode. Substrate is SiO_2 (100 nm)/Si. The Ti layer is 3 nm thick.

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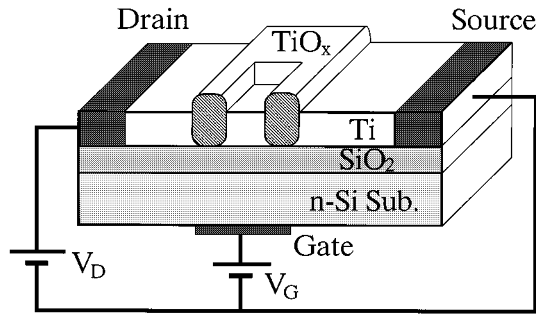

FIG. 2. Cross-sectional view of single electron transistor fabricated by STM nano-oxidation process. Island area is surrounded by two TiO_x line and two large TiO_x barrier regions.

diode measured at 103 K is shown in Fig. 4. This diode has two tunnel junctions made by TiO_x narrow line, and does not have the gate electrode. The current was measured between the source and drain electrode. In the figure, the thick line shows the current of the diode, and the fine line shows the differential of the current, i.e., the conductance of the diode. At around the zero drain voltage, the current shows no increase with the increase of the drain voltage, meaning the existence of the Coulomb gap. The Coulomb gap voltage is about 50 mV. At the drain voltage larger than the Coulomb gap voltage, the current increases rapidly. The conductance shows the lowest peak at around the zero drain voltage and is almost zero (S), which corresponds to the Coulomb gap. At the drain voltage larger than the Coulomb gap voltage, the conductance shows the weak oscillation with the increase of the drain voltage. The lower peaks of the conductance oscillation, e.g., at $V_D = \sim 0.1$ or ~ 0.28 V, indicate that there are Coulomb staircases in the current. However, in this diode, the clear Coulomb staircase could not be observed. This may be attributed to the symmetrical size and characteristics of the two tunnel junctions, i.e., the same tunneling resistances and the same tunneling capacitances made by the STM nano-oxidation process.

The drain current–voltage characteristics of the SET was measured at room temperature and is shown in Fig.5. The gate bias was set to 2 V. In the figure, the thick line shows the current of the SET, and the fine line the conductance of the SET. Between the drain bias of 0 and -0.75 V, four clear Coulomb staircases with the ~ 150 mV period are observed.

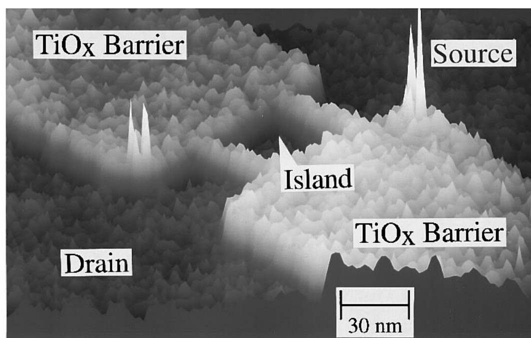

FIG. 3. Atomic force microscope (AFM) image of island region of fabricated SET.

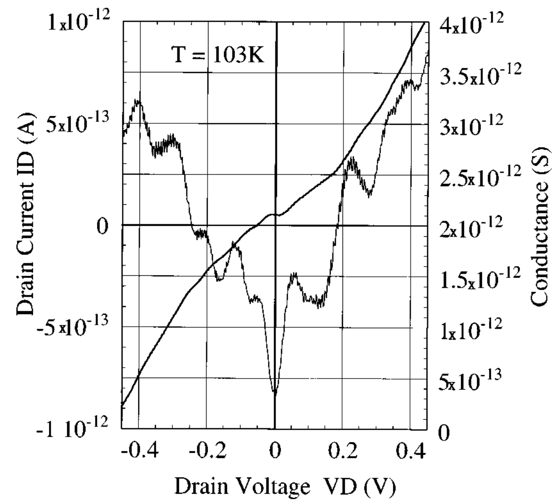

FIG. 4. Drain current–voltage characteristics (thick line) and conductance (fine line) of diode at $T = 103$ K. Coulomb gap of ~ 50 mV is observed around drain bias of 0 V. Conductance oscillates with increase of drain voltage meaning the existence of Coulomb staircase.

The conductance oscillates with the increase of the drain bias with almost the same periods of ~ 150 mV. The lower peaks of the conductance oscillation correspond to the flat regions of the current of the Coulomb staircase.

The Coulomb staircase shown in Fig. 5 may be attributed to the asymmetrical structure of the two tunneling junctions. One TiO_x tunneling junction of the SET in Fig. 5 has a width of 18 nm, while the other tunneling junction is 27 nm. Due to this difference in the tunneling junction width, each tunneling junction has the different values of the conductances and capacitances, which produces the Coulomb staircase.

Each height of the Coulomb staircase in Fig. 5 becomes larger at the larger drain voltage. This may be attributed to the increase of the tunneling probability of the electron through the TiO_x tunneling barrier. Because the height of the

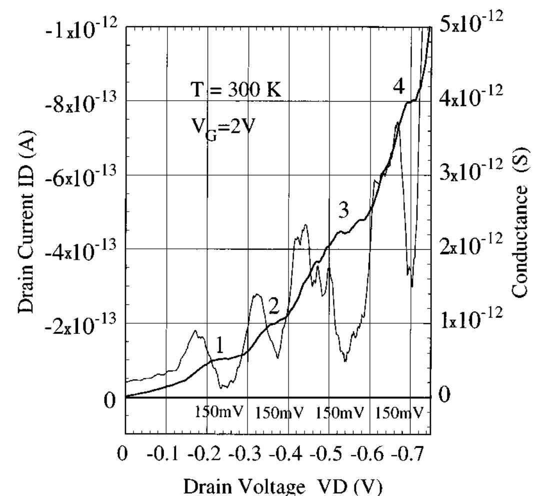

FIG. 5. Drain current–voltage characteristics (thick line) and conductance (fine line) of SET at room temperature. Gate bias is set to 2 V. Four clear Coulomb staircases of ~ 150 mV period are obtained even at room temperature.

TiO_x tunneling barrier lowered by the applied drain bias and the Fowler–Nordheim tunneling current increases.

The dependence of the drain current on the gate bias was also examined at room temperature with the drain bias of 150 mV, and it exhibits clear current oscillations with a period of ~460 mV, implying a periodic Coulomb oscillation of the current. The tunneling capacitance, C_t, and gate capacitance, C_g, could be roughly estimated from the period of the Coulomb staircase and the Coulomb oscillation and are $C_t = \sim 3.6 \times 10^{-19}$ F and $C_g = \sim 3.5 \times 10^{-19}$ F, respectively. These estimated values of the capacitances obtained from the I–V characteristics of the SET coincide well with the calculated capacitances from its structural parameters. These results confirm the existence of Coulomb blockade phenomena at room temperature due to the small dimension of the island in the SET made by the STM nano-oxidation process.

In conclusion, we have succeeded in the fabrication of the single electron transistor using the STM nano-oxidation process, and the SET was operated at room temperature. The single electron diode shows the Coulomb gap of about 50 mV at the temperature of 103 K, and the SET shows the Coulomb staircase with the periods of 150 mV at the temperature of 300 K. These Coulomb gap and Coulomb staircase observed at the high temperature are attributed to the small tunneling junction area made by the STM nano-oxidation process. The STM nano-oxidation process is quite easy and could be applicable to any kinds of devices. We open the new frontier where the new nanometer size device processing makes the SET possible to work at room temperature.

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