

# Resumé

## Personal Information

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**Sex** : Male  
**Marital status** : Single  
**Nationality** : Indian  
**Date of Birth** : Feb 25, 1984

## Academic Record

**Educational Status** : First Year of Masters of Science at  
Department of Electrical & Computer Engineering  
Rice University  
Awarded Bachelor of Technology Degree at  
Department of Computer Science & Engineering  
Indian Institute of Technology, Bombay

| <b>School/University</b>                 | <b>Degree/<br/>Certificate</b> | <b>Date of<br/>award</b> | <b>% Marks/<br/>GPA</b> |
|--|--------------------------------|--------------------------|-------------------------|
| Indian Institute of Technology<br>Bombay | Bachelor of<br>Technology      | June 2005                | 8.83/10                 |
| Maharashtra State Board                  | (Class XII)                    | June 2001                | 94%                     |
| Central Board for Secondary<br>Education | (Class X)                      | June 1999                | 88.8%                   |

## Academic Honors

- Represented IIT Bombay in All India Intel Student Research Contest 2004 and was awarded **2nd RunnerUp among 16 top universities in India including IITs**. It was a 1-year research project in collaboration with mentors from Intel on "Generation of Test Vectors for SRAM-based FPGAs under Multiple Fault Model".
- Ranked 67<sup>th</sup> among approximately 150,000 examinees in JEE 2001, the Joint Entrance Examination for admission to the IITs.
- Ranked 25<sup>th</sup> among approximately 100,000 examinees in IIIT, Hyderabad Entrance Examination 2001.
- Recipient of the prestigious National Talent Search Scholarship awarded by Govt. of India.
- Selected among the top 35 students in the Indian National Physics Olympiad (IN-PhO), 2001, and attended a 25-day training camp for selecting the Indian contingent to participate in the International Physics Olympiad (IPhO). Awarded the NSEP Gold medal for this achievement.
- Qualified to appear in the Indian National Chemistry Olympiad in 2001 (INChO-2001) through a nation-wide screening test, National Standard Examination in Chemistry. Awarded a Certificate of Merit for this achievement.
- Represented Mumbai region in the Indian National Mathematics Olympiad (INMO-1999). Only 30 students were selected from the entire region to represent it, and about 480 throughout India. I was ranked 12<sup>th</sup> among the thirty selected.
- Secured 12<sup>th</sup> rank in Merit List of Maharashtra Board in +2 examination 94% aggregate.
- Secured 33<sup>rd</sup> rank in All India Talent Search Exam, 2000-2001.

## Publications

1. "Multiple Fault testing of Logic Resources of SRAM-Based FPGAs", 18<sup>th</sup> International Conference on VLSI Design, 4<sup>th</sup> International Conference on Embedded Systems Jan.3-7, 2005, Kolkatta, India.

## Research Experience

### • Senior Thesis

Currently, I am working on my BTech. Project on "Converting Synchronous circuits to Asynchronous circuits" under Prof. S. S. S. P. Rao. The aim is to develop a tool which can convert a synchronous circuit to an asynchronous circuit by eliminating the global clock and adding control circuitry which generate local clocks for synchronous islands.

### • Summer Training / Work Experience

During Summer'2003, I did my internship at Intel Bangalore, India. The project was on "Switch level simulation of circuits". I studied and suggested optimizations in a tool developed at Intel. This tool used a Symbolic MOS analyzer tool, ANAMOS developed at CMU. The internship was for a period of 10 weeks.

- **Seminar (Junior Thesis)**

In my junior year, I worked on “Multiple fault testing of SRAM-based FPGAs”, under the guidance of Prof. S. S. S. P. Rao. During this time, I did a comprehensive study of various methodologies for testing digital circuits and FPGAs. The work done in the seminar has been published in the paper mentioned above.

- **Summer Project**

During Summer’ 2002, I did a summer project at IIT Bombay, under Prof. S. S. S. P. Rao. The project was on building an interface for a printer that would enable the printer to be connected directly to the LAN, instead of connecting it through a PC. The implementation of the receiver unit was done using FPGAs and VHDL. It was tested using a Xilinx 3000 Demo board.

- **Microprocessor Project:**

Designed and implemented 4-bit microprocessor having five instructions. The implementation was done in two ways:

1. Using SSI,MSI components (AND, OR gates) and a binary adder chip.
2. Using VHDL, on an FPGA.

Both these projects were a part of the Microprocessor course in the 5<sup>th</sup> and 6<sup>th</sup> semesters.

- **AI Project and Seminar (Spring 2004)**

During my junior year, I studied different approaches for generalized graph search including algorithms for performing Real Time search, and demonstrated their applications in a seminar. Working in a group of four we implemented these algorithms, in a GUI based tool for simulating the game Chinese Checker. This project was done under the guidance of Prof. Pushpak Bhattacharya.

- **Distributing the Optimum Golomb Ruler search (Autumn 2002)**

Improved the shift algorithm (standard algorithm for OGR search) and customized it for processing over a distributed network. Controlled the number of processes spawned and process size based on experimental statistical data to minimize communication overheads. This project was done under the guidance of Dr. S Arunkumar.

#### Projects Undertaken

- **Logic Design Project:** Designed and implemented a binary multiplier using FPGAs.
- **Compilers Project:** Writing a compiler for a subset of Pascal using C, Lex and Yacc.
- **Asynchronous Design Project:** Modelling a GasP cell using Uppaal. It was a part of Asynchronous designs course.
- **Software Systems Project:** The project was to study a large software and make improvements in it. Our project was on the “Network Pathology Tool”. When this tool is run on a terminal in a network, it detects the topology of the network. We made improvements like wild card IP and MAC address searches.

Some of the above were part of labs and courses and were done in groups.

#### Software Exposure

I am well conversant with the following programming languages: **C++**, **Pascal**, and **Java**. I am also quite comfortable with: **C**, **Prolog** and **Scheme**.

I have worked extensively on, and am well conversant with the following platforms: DOS, UNIX, SunOS and Linux. I am also quite comfortable with Windows NT and Windows 95.

#### Extra Curricular Activities

1. Runner Up in All India CBSE Schools TT Tournament representing Atomic Energy Central School, Bombay.
2. Represented the Hostel in Inter hostel TT tournament.
3. Awarded Hostel Special Mention for performance in Sports.
4. Nominated as the Hostel System Administrator for 2003-04.

Declaration I hereby declare that the information given above is true to the best of my knowledge.

(Mihir Choudhury)

Date