Challenges to Crossbar Integration of Nanoscale Two-Terminal Symmetric Memory Devices

Mian Dong and Lin Zhong
Department of Electrical and Computer Engineering
Rice University
Houston, TX, USA
{dongmian; lzhong}@rice.edu

***Abstract*—Crossbar is the most efficient architecture to organize memory devices into dense, large-scale arrays. Emerging nanotechnology promises two-terminal, symmetric memory devices of superior electrical properties. In this work, however, we show that these two-terminal, symmetric devices impose grave challenges to the crossbar-based memory organization. First, we prove that conventional crossbar organization will not work for such symmetric devices. Second, we propose a revised crossbar organization that does work for such devices. However, diodes or switches must be employed to convert such devices into asymmetrical devices in order to avoid considerable energy cost, which can significantly discount their advantage over conventional asymmetrical devices. Third, we demonstrate that there is significant difference in delay and power consumption for accessing a memory device of different contents, i.e., 0 or 1. Such difference constitutes a performance bottleneck of crossbar-based integration of resistive memory devices.**

Keywords-crossbar; memory device; nanotechnology

I. INTRODUCTION AND BACKGROUND

Crossbar is widely used for integrating memory devices into dense, large-scale arrays, due to many desirable properties. First, its periodic geometry facilitates large-scale, even three-dimension fabrication [1]. Second, it defines devices and interconnects in such a compact form that ultra-high density is possible [2]. Third, it provides very efficient means to address every memory device in the array through either two-terminal or one terminal addressing mechanisms, as illustrated in Figure 1. In two-terminal addressing, the two terminals of a memory device are selected by two different wires (X or Y), as shown in Figure 1 (a); in one-terminal addressing, one terminal of the memory device is connected to a common wire (C) shared by all the memory devices, and the other terminal is selected by two wires (X and Y), as shown in Figure 1 (b). One-terminal addressing, e.g. as in DRAM, is usually implemented with MOSFET, which is the major obstacle to a higher memory density. Therefore, we only consider two-terminal addressing in this work.

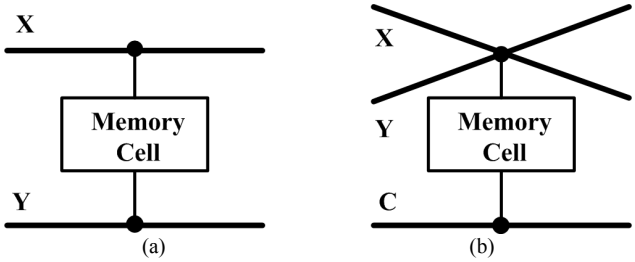

Figure 1. Memory device addressing; (a) two-terminal addressing; (b) one-terminal addressing.

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We can model a two-terminal memory device as a resistor (*R*) and a diode (*D*), illustrated in Figure2. The resistor has two states, i.e., high resistance (HR) state and low resistance (LR) state, which can represent one bit of information. The diode indicates that current flows asymmetrically, i.e., only from one terminal to the other but not backward. By applying a voltage between the two terminals of a memory device (the dark grey one), we are able read out the information of it by sensing the amplitude of the current flowing through it.

However, emerging nanotechnology provides us symmetric devices in which current can go in both directions [3]. Such symmetric devices promise superior electrical properties in on-off ratio, read/write speed, and power consumption. However, they impose grave challenges to the crossbar-based integration, as detailed below.

II. TECHINICAL CONTRIBUTIONS

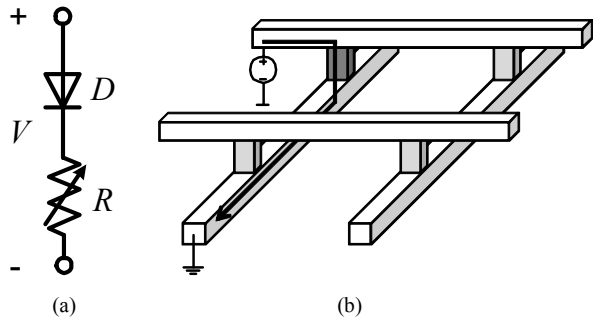

Figure 2. (a) A two-terminal asymmetric memory device; (b) A 2×2 crossbar of asymmetric memory devices. By applying a voltage and sensing the current (the black solid arrow), we can read out the information stored in the dark grey device.

First, we prove that the two-terminal addressing does not work in a conventional crossbar of symmetric memory devices and every device must be asymmetric to make the crossbar memory array functions correctly. This is apparent for a 2×2 crossbar. Suppose a memory device is symmetric, say the white one in Figure 3. When we read the dark grey device, there will be an extra current (the grey dashed arrow) to interfere the current we need to sense (the black solid arrow) and we will read out a wrong value. Thus, every device in a 2×2 crossbar must be asymmetric. Then we can easily extend the same conclusion to a crossbar of any scale, because every device in a 2×2 sub-crossbar must be asymmetric. Therefore, two terminal symmetric memory devices cannot be used directly in a crossbar memory. Even worse, the grounded solution proposed in [4] does not work in this case either. To make it work, we should use a diode of switch to make the symmetric memory device behave asymmetrically.

Second, we can revise the two-terminal addressing mechanism so that it works for crossbar of symmetric memory devices by dynamically assigning proper voltages to the wires in the crossbar, as illustrated in Figure 4. Unfortunately, this solution suffers from considerable energy waste. As shown in Figure 4, there will be a current going through each device with a circle. If we only read one device at a time, e.g., the one with a solid circle, the currents through other devices with dashed circles will contribute to significant energy waste.

Third, we demonstrate the crossbar organization is subject to significant difference in access power and delay, depending on the content of the accessed memory device. Figure 5 shows the equivalent circuit of a crossbar memory. It shows that the delay to access a memory device is affected not only by the position (x and y), but also by the content (R) of the memory device.

Since the clock rate of the memory is determined by the delay in the worst case, the difference constitutes a bottleneck to enhancing memory speed. Same is true for the power consumption of accessing a memory device. As shown in Figure 6, the power consumption of accessing a memory device of state LR is higher than the one to read a memory device of state HR. And the difference can be considerable if the memory device has a high on/off ratio (R_H/R_L), which is usually desirable. This difference will lead to a considerable power waste if most of the memory devices are in state LR.

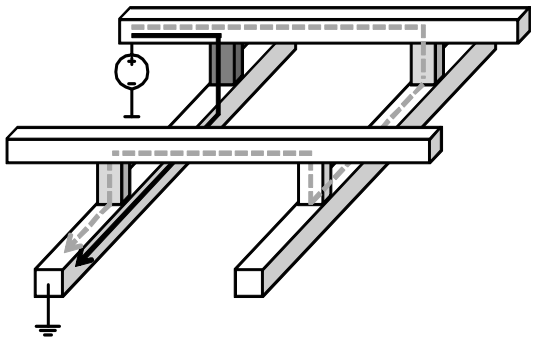

Figure 3. Two-terminal addressing does not function correctly in a 2×2 crossbar of symmetric memory devices. Because the white device is symmetric, an extra current (the grey dashed arrow) will interfere the current we need to sense (the black solid arrow) and we will get a wrong content of the dark grey device.

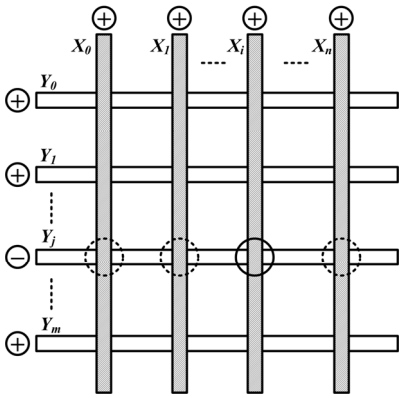

Figure 4. Proper voltage assignment (positive: voltage source; negative: ground) makes a crossbar with symmetric memory devices function correctly. By sensing the current flowing from X_i to Y_j at the terminal X_i, we can read out the information stored in the device with the solid circle. There also exist other currents such as the one from X_0 to Y_j and the one from X_i to Y_j, which will lead to not an error but a significant energy waste.

III. CONCLUSION

In this work, we show that two-terminal symmetric memory devices cannot be directly integrated using a crossbar. We suggest revisions to the conventional addressing mechanism and point out their limitations as well. Our work not only sheds insight into crossbar architecture and memory organization, but also indicates real implementation challenges for integrating emerging two-terminal nanoscale memory devices. Our work also provides the foundation for overcoming these challenges through system, architectural, and circuit innovations.

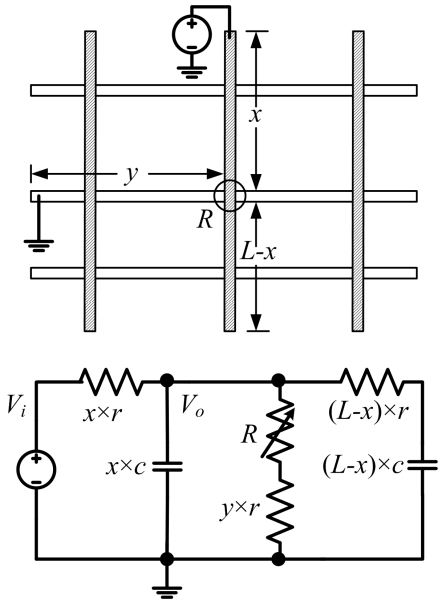

Figure 5. Equivalent circuit of a crossbar memory, where L is the length of a wire, r is unit resistance of a wire, c is unit capacitance of a wire. The delay to access the device with solid circle is affected not only by the position (x, y), but also by the content (R) of the device.

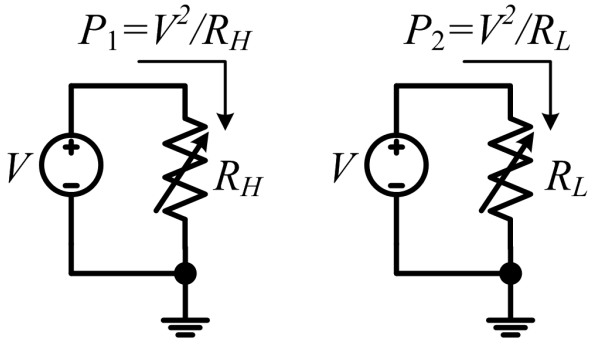

Figure 6. The power consumption of accessing a device in HR state (R_H) and a device in LR state (R_L) is P_1 and P_2, respectively. When R_H /R_L is high enough, the difference between P_1 and P_2 will be significant.

ACKNOWLEDGMENT

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